Description

THIN FILM DIODE PANEL AND MANUFACTURING METHOD OF THE SAME

Technical Field

[1] The present disclosure relates to thin film diode array panels using metal insulator metal (MIM) diodes as switching elements, and a manufacturing method of the same. In more detail, the present disclosure relates to thin film diode array panels of a dual select diode (DSD) type, and a liquid crystal display using the same.

Background Art

[2] A liquid crystal display (LCD) is one of the most widely used flat panel displays. An LCD includes two panels provided with field-generating electrodes, and a liquid crystal (LC) layer interposed therebetween. The LCD displays images by applying voltages to the field-generating electrodes to generate an electric field in the LC layer, which determines orientations of LC molecules in the LC layer to adjust polarization of incident light.

[3] An LCD may have switching elements to switch voltages of pixels arranged in a matrix form. An LCD can display various images since pixel voltages are individually switched. An LCD having switching elements to switch pixel voltages individually is called an active matrix LCD.

[4] Thin film transistors or thin film diodes may be used as the switching elements. When thin film diodes are applied, MIM diodes can be used.

[5] A MIM diode has two metal layers and one insulating layer interposed between the metal layers, and a thickness capable of being measured in micrometers. A MIM diode may act as a switch due to electrical non-linearity of the insulating layer. A MIM diode has two terminals, and as a result, the manufacturing process of the MIM diode is simpler than that of the thin film transistor having three terminals. Accordingly, MIM diodes can be manufactured at a lower cost than thin film transistors.

[6] However, when diodes are used as switching elements, the uniformity of image quality and contrast ratio may be degraded due to asymmetry of an applied voltage with respect to the polarity.

[7] In response to the asymmetry, a dual select diode (DSD) panel has been developed. A DSD panel includes two diodes that are symmetrically connected to a pixel electrode and are driven by applying voltages of opposite polarities.

[8] A DSD LCD shows improved image quality, contrast ratio, gray scale uniformity,

and response speed by applying voltages having opposite polarities to two diodes that are connected to the same pixel electrode. Accordingly, a DSD type LCD can display images with high resolution like that of an LCD using thin film transistors.

[9] A thin film diode array panel of a conventional DSD LCD has transmission electrodes made of a transparent conductor such as indium tin oxide (ITO) formed on a substrate as a bottom layer, and signal lines made of a metal and formed on the other layers as a top layer.

Disclosure of Invention

Technical Problem

[10] Hence, such a conventional thin film diode array panel structure has demerits as follows.

[11] It is difficult to manufacture the thin film diode array panel by using a mass production line for manufacturing a thin film transistor array panel.

[12] There is a large possibility of having a signal line defect because metal signal lines which are chemically weak are exposed to a liquid crystal material and external environments.

[13] Off current (Ioff) of a MIM diode is increased because back light reaches the silicone-rich silicon nitride (Si-rich SiNx) layer that forms a channel of the MIM diode, and activates the Si-rich SiNx layer. To solve such a problem, the back light unit is disposed on the color filter panel side and displayed images are seen in front of the thin film diode panel. However, this method also has problems such that characteristics of MIM diodes are affected by external light, and the contrast ratio is degraded due to light reflections by the metal signal lines.

Technical Solution

[14] The present invention provides a thin film diode array panel comprising: an insulating substrate; first and second redundant gate lines made of an opaque conductor and formed on the insulating substrate; first and second floating electrodes made of an opaque conductor, formed on the insulating substrate and disposed between the first and second redundant gate lines; an insulating layer formed on the first and second floating electrodes; a first gate line formed on the first redundant gate line and including a first input electrode overlapping the first floating electrode where the insulating layer is interposed between the first input electrode and the first floating electrode; a second gate line formed on the second redundant gate line and including a second input electrode overlapping the second floating electrode where the insulating

layer is interposed between the second input electrode and the second floating electrode; and a pixel electrode including a first contact electrode overlapping the first floating electrode where the insulating layer is interposed between the first contact electrode and the first floating electrode, a second contact electrode overlapping the second floating electrode where the insulating layer is interposed between the second contact electrode and the second floating electrode, and a main body.

[15] Here, the first and second redundant gate lines and the first and second floating electrodes may be made of Mo, and the pixel electrode and the first and second gate lines may be made of ITO. The insulating layer may include a first insulating layer regionally formed around the first floating electrode, and a second insulating layer regionally formed around the second floating electrode. The insulating layer may cover the first and second redundant gate lines and the first and second floating electrodes and may have contact holes exposing the first and second redundant gate lines, and the first and second gate lines may be connected to the first and second redundant gate lines through the contact holes. The insulating layer may cover the first and second redundant gate lines and the first and second floating electrodes and may have cutout stripes exposing the first and second redundant gate lines, and the first and second gate lines may be connected to the first and second redundant gate lines through the cutout stripes. The insulating layer may have a cutout disposed to overlap at least a portion of the main body of the pixel electrode. The cutout may be disposed under the main body of the pixel electrode and expose a portion of the insulating substrate around the main body of the pixel electrode.

[16] A thin film diode array panel comprising: an insulating substrate; first redundant gate lines including a first input electrode and made of an opaque conductor; second redundant gate lines including a second input electrode and made of an opaque c onductor; first and second contact electrodes formed on the insulating substrate and made of an opaque conductor; an insulating layer formed on the first and second input electrodes and the first and second contact electrodes; a first gate line formed on the first redundant gate line; a second gate line formed on the second redundant gate line; a first floating electrode formed on the insulating layer and overlapping the first input electrode and the first contact electrode; a second floating electrode formed on the insulating layer and overlapping the second input electrode and the second contact electrode; and a pixel electrode connected to the first and second contact electrodes, is provided.

[17] The first and second redundant gate lines and the first and second contact electrodes

may be made of Mo, and the pixel electrode and the first and second gate lines may be made of ITO. The insulating layer may include a first insulating layer regionally formed around the first floating electrode, and a second insulating layer regionally formed around the second floating electrode. The insulating layer may cover the first and second redundant gate lines and the first and second contact electrodes and may have contact holes exposing the first and second redundant gate lines, and the first and second gate lines may be connected to the first and second redundant gate lines through the contact holes. The insulating layer may cover the first and second redundant gate lines and the first and second contact electrodes and may have cutout stripes exposing the first and second redundant gate lines, and the first and second gate lines may be connected to the first and second redundant gate lines through the cutout stripes. The insulating layer may have a cutout disposed to overlap at least a portion of the main body of the pixel electrode. The cutout is disposed under the main body of the pixel electrode, and exposes a portion of the insulating substrate around the main body of the pixel electrode.

Advantageous Effects

[18] According to the present invention, since signal lines made of a chemically weak metal are covered and protected by an insulating layer and transparent electrode, the possibility of signal line defects is diminished. Since a metal layer intercepts light, even though a back light is disposed under the thin film diode panel, off current (Ioff) of the MIM diodes is not increased.

Brief Description of the Drawings

[19] Preferred embodiments of the present invention can be understood in more detail from the following descriptions taken in conjunction with the accompanying drawings, in which:

[20] Fig. 1 is a perspective view of a liquid crystal display according to an embodiment of the present invention;

[21] Fig. 2 is a layout view of a thin film diode array panel for a liquid crystal display according to an embodiment of the present invention;

[22] Fig. 3 is a sectional view of the thin film diode array panel taken along the line III-III of Fig. 2;

[23] Fig. 4 is a layout view of a thin film diode array panel in an intermediate step of manufacturing the thin film diode array panel of Figs. 2 and 3;

[24] Fig. 5 is a sectional view of the thin film diode array panel shown in Fig. 4 taken

along the line V-V

[25] Fig. 6 is a layout view of a thin film diode array panel in the next step of Figs. 4 and 5 of manufacturing the thin film diode array panel of Figs. 2 and 3;

[26] Fig. 7 is a sectional view of the thin film diode array panel shown in Fig. 6 taken along the line VII-VII

[27] Fig. 8 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention;

[28] Fig. 9 is a sectional view of the thin film diode array panel taken along the line IX-IX of Fig. 8;

[29] Fig. 10 is a layout view of a thin film diode array panel in an intermediate step of manufacturing the thin film diode array panel of Figs. 8 and 9;

[30] Fig. 11 is a sectional view of the thin film diode array panel shown in Fig. 10 taken along the line XI-XI

[31] Fig. 12 is a layout view of a thin film diode array panel in the next step of Figs. 11 and 12 of manufacturing the thin film diode array panel of Figs. 8 and 9;

[32] Fig. 13 is a sectional view of the thin film diode array panel shown in Fig. 12 taken along the line XIII-XIII

[33] Fig. 14 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention;

[34] Fig. 15 is a sectional view of the thin film diode array panel taken along the line XV-XV of Fig. 14;

[35] Fig. 16 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention;

[36] Fig. 17 is a sectional view of the thin film diode array panel taken along the line XVII-XVII of Fig. 16;

[37] Fig. 18 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention;

[38] Fig. 19 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention;

[39] Fig. 20 is a sectional view of the thin film diode array panel taken along the line XX-XX of Fig. 19;

[40] Fig. 21 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention;

[41] Fig. 22 is a sectional view of the thin film diode array panel taken along the line XXII-XXII of Fig. 21; and

[42] Fig. 23 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention.

Best Mode for Carrying Out the Invention

[43] Preferred embodiments of the present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[44] In the drawings, the thickness of layers, films, and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

[45] Fig. 1 is a perspective view of a liquid crystal display according to an embodiment of the present invention.

[46] As shown in Fig. 1, the liquid crystal display has a lower panel (a thin film diode array panel) 100, an upper panel (a color filter array panel) 200 facing the lower panel 100, and a liquid crystal layer 3 interposed between the two panels 100 and 200 and having liquid crystal molecules aligned in a horizontal direction with respect to the surfaces of the panels 100 and 200.

[47] The lower panel 100 has a plurality of pixel electrodes 190 formed on corresponding regions with red, green, and blue pixels; a plurality of pairs of gate lines 121 and 122 transmitting signals having opposite polarities; and a plurality of MIM diodes D1 and D2 which are switching elements.

[48] The upper panel 200 includes a plurality of data electrode lines 230 forming an electric field along with the pixel electrode 190 for driving liquid crystal molecules and defining pixel regions by intersecting the pairs of gate lines 121 and 122, and a plurality of red, green, and blue color filters 220 which respectively correspond with pixel areas to define red, green, and blue pixel areas. White pixel areas on which no color filter is formed may be included.

[49] Henceforth, a structure of a thin film diode array panel 100 according to an embodiment of the present invention will be described in detail.

[50] Fig. 2 is a layout view of a thin film diode array panel for a liquid crystal display

according to an embodiment of the present invention, and Fig. 3 is a sectional view of the thin film diode array panel taken along the line III-III of Fig. 2 according to an embodiment of the present invention.

[51] As shown in Figs. 2 and 3, first and second redundant gate lines 141 and 142 and first and second floating electrodes 143 and 144 are formed on an insulating substrate 110 made of a transparent insulating material such as glass. The first and second floating electrodes 143 and 144 are disposed between the first and second redundant gate lines 141 and 142. The first and second redundant gate lines 141 and 142 and first and second floating electrodes 143 and 144 are made of an opaque conductor such as molybdenum (Mo), aluminum (Al), tantalum (Ta), titanium (Ti), and their alloys.

[52] First and second insulating layers 151 and 152 are respectively formed on the first and second floating electrodes 143 and 144. The first and second insulating layers 151 and 152 are made of silicon nitride (SiNx). The first and second insulating layers 151 and 152 have boundaries around the first and second floating electrodes 143 and 144.

[53] A plurality of pixel electrodes 190 having first and second contact portions 191 and 192 and a plurality of first and second gate lines 121 and 122 respectively having first input electrodes 123 and second input electrodes 124 are formed on the first and second insulating layers 151 and 152. The pixel electrodes 190 and the first and second gate lines 121 and 122 are made of a transparent conductor such as ITO and IZO.

[54] The main body of the pixel electrode 190 contacts the insulating substrate 110. The first contact portion 191 contacts the first insulating layer 151 and overlaps the first floating electrode 143. The second contact portion 192 contacts the second insulating layer 152 and overlaps the second floating electrode 144.

[55] The first and second gate lines 121 and 122 respectively cover the first redundant gate lines 141 and the second redundant gate lines 142. The first input electrode 123 contacts the first insulating layer 151 and overlaps the first floating electrode 143. The second input electrode 124 contacts the second insulating layer 152 and overlaps the second floating electrode 144.

[56] The input electrodes 123 and 124, the insulating layers 151 and 152, the floating electrodes 143 and 144, and the contact portions 191 and 192 form two MIM diodes.

[57] Due to the nonlinearity of voltage-current characteristics of the insulating layer 151 and 152, the MIM diodes permit the pixel electrode 190 to be charged only when a voltage greater than the critical voltage of the insulating layers 151 and 152 is applied. On the contrary, when no signal voltage is applied to the MIM diodes, the charged voltage is preserved in a liquid crystal capacitor formed between the pixel electrode

190 and a data electrode line 230, since the channels of the MIM diodes are closed.

[58] An LCD using a thin film diode array panel of Figs. 2 and 3 has a wider aperture ratio than an LCD using TFTs to enhance brightness.

[59] Since the floating electrodes 143 and 144 made of an opaque metal are disposed on the insulating substrate 110 as a bottom layer and the insulating layers 151 and 152 are formed on the floating electrodes 143 and 144, even though a back light is disposed under the thin film diode panel 100, the light of the back light does not reach the insulating layers 151 and 152 due to interception of the floating electrodes 143 and 144. As a result, off current (Ioff) of the MIM diodes is not increased.

[60] Since the floating electrodes 143 and 144 and the first and second redundant gate lines 141 and 142 made of a chemically weak metal are covered and protected by the insulating layers 151 and 152 and the first and second gate lines 121 and 122, the possibility of signal line defects decreases.

[61] Henceforth, a manufacturing method of a thin film diode array panel according to an embodiment of the present invention will be described.

[62] Fig. 4 is layout view of a thin film diode array panel in an intermediate step of manufacturing the thin film diode array panel of Figs. 2 and 3; Fig. 5 is a sectional view of the thin film diode array panel shown in Fig. 4 taken along the line V-V Fig. 6 is a layout view of a thin film diode array panel in the next step of Figs. 4 and 5 of manufacturing the thin film diode array panel of Figs. 2 and 3; and Fig. 7 is a sectional view of the thin film diode array panel shown in Fig. 6 taken along the line VII-VII

[63] As shown in Figs. 4 and 5, a metal layer made of an opaque metal such as Mo, Al, Ta, Ti, and their alloys is deposited on the insulating substrate 110 and is photo-etched to form the first and second redundant gate lines 141 and 142 and first and second floating electrodes 143 and 144.

[64] Next, a silicon nitride layer is deposited and is photo-etched to form the first insulating layer 151 on the first floating electrode 143 and to form the second insulating layer 152 on the second floating electrode 144.

[65] Next, as shown in Figs. 2 and 3, an ITO layer is deposited on the first and second insulating layers 151 and 152 and is photo-etched to form the pixel electrode 190 having the first and second contact portions 191 and 192 and the first and second gate lines 121 and 122 respectively including the first and second input electrodes 123 and 124.

[66] Another embodiment of the present invention will now be described.

[67] Fig. 8 is a layout view of a thin film diode array panel for a liquid crystal display

according to another embodiment of the present invention, and Fig. 9 is a sectional view of the thin film diode array panel taken along the line IX-IX of Fig. 8.

[68] As shown in Figs. 8 and 9, first and second redundant gate lines 141 and 142 substantially extending in a transverse direction are formed on an insulating substrate 110 made of a transparent insulating material such as a glass. The first and second redundant gate lines 141 and 142 respectively include a plurality of first and second input electrodes 145 and 146 protruding in a longitudinal direction.

[69] A first and second contact electrodes 147 and 148 having a shape of the character are formed on the insulating substrate 110. The first contact electrode 147 is adjacent to the first input electrode 145, and the second contact electrode 148 is adjacent to the second input electrode 146.

[70] The first and second redundant gate lines 141 and 142, the first and second input electrodes 145 and 146, and the first and second contact electrodes 147 and 148 are made of an opaque conductor such as molybdenum (Mo), aluminum (Al), tantalum (Ta), titanium (Ti), and their alloys.

[71] First and second insulating layers 151 and 152 are respectively formed on the first input electrode 145 and the first contact electrode 147 and on the second input electrode 146 and the second contact electrode 148. The first and second insulating layers 151 and 152 are made of silicon nitride (SiNx). The first and second insulating layers 151 and 152 have boundaries around the first input electrodes 145 and the first contact electrode 147 and around the second input electrdoe146 and the second contact electrode 148.

[72] First and second gate lines 121 and 122 and first and second floating electrodes 125 and 126 are formed on the first and second insulating layers 151 and 152. A pixel electrode 190 is formed on the first and second insulating layers 151 and 152 to contact with the exposed portion of the first and second contact electrodes 147 and 148.

[73] The pixel electrodes 190, the first and second gate lines 121 and 122, and the first and second floating electrodes 125 and 126 are made of a transparent conductor such as an ITO and IZO.

[74] The first floating electrode 125 overlaps the first input electrodes 145 and the first contact electrode 147. The second floating electrode 126 overlaps the second input electrode 146 and the second contact electrode 148.

[75] The first and second gate lines 121 and 122 respectively cover the first redundant gate lines 141 and the second redundant gate lines 142.

[76] The pixel electrode 190 mainly contacts the insulating substrate 110, covers the exposed portions of the first and second contact electrodes 147 and 148, and partially contacts the first and second insulating layer 151 and 152. Accordingly, the first and second contact electrodes 146 and 147 are covered and protected by the first and second insulating layers 151 and 152 and the pixel electrode 190.

[77] The input electrodes 145 and 146, the insulating layers 151 and 152, the floating electrodes 125 and 126, and the contact electrodes 147 and 148 form two MIM diodes.

[78] An LCD using a thin film diode array panel of Figs. 8 and 9 has a wider aperture ratio than an LCD using TFTs to enhance brightness.

[79] Since the input electrodes 145 and 146 made of an opaque metal are disposed on the insulating substrate 110 as a bottom layer and the insulating layers 151 and 152 are formed on the floating electrodes 143 and 144, even though a back light is disposed under the thin film diode panel 100, the light of the back light does not reach the insulating layers 151 and 152 due to interception of the input electrodes 145 and 146. As a result, off current (Ioff) of the MIM diodes is not increased

[80] Since the contact electrodes 147 and 148 and the redundant gate lines 141 and 142 made of a chemically weak metal are covered and protected by the insulating layer 151 and 152 and the first and second gate lines 121 and 122, the possibility of signal line defects decreases.

[81] Hence, a manufacturing method of a thin film diode array panel according to an embodiment of the present invention will be described.

[82] Fig. 10 is layout view of a thin film diode array panel in an intermediate step of manufacturing the thin film diode array panel of Figs. 8 and 9; Fig. 11 is a sectional view of the thin film diode array panel shown in Fig. 10 taken along the line XI-XI Fig. 12 is a layout view of a thin film diode array panel in the next step of Figs. 11 and 12 of manufacturing the thin film diode array panel of Figs. 8 and 9; and Fig. 13 is a sectional view of the thin film diode array panel shown in Fig. 12 taken along the line XIII-XIII

[83] As shown in Figs. 10 and 11, a metal layer made of an opaque metal such as Mo, Al, Ta, Ti, and their alloys is deposited on the insulating substrate 110, and is photo-etched to form the first and second redundant gate lines 141 and 142 and first and second contact electrodes 147 and 148.

[84] Next, as shown in Figs. 12 and 13, a silicon nitride layer is deposited and is photo-etched to form the first insulating layer 151 on the first input electrode 145 and the first contact electrode 147, and to form the second insulating layer 152 on the second input

electrode 146 and the second contact electrode 148.

[85] Next, as shown in Figs. 8 and 9, an ITO layer is deposited on the first and second insulating layers 151 and 152 and is photo-etched to form the pixel electrode 190 and the first and second floating electrode 125 and 126.

[86] In the above describe embodiment, the insulating layers are regionally disposed around the floating electrode. However, the shape of the insulating layers may be changed in various ways. Such variations will be described as other embodiments.

[87] Fig. 14 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention, and Fig. 15 is a sectional view of the thin film diode array panel taken along the line XV-XV of Fig. 14.

[88] When the thin film diode array panel of Figs. 14 and 15 is compared with that of Figs. 2 and 3, the shape of an insulating layer 150 is different.

[89] That is, the insulating layer 150 is formed on the entire area of the insulating substrate 110 to cover the redundant gate lines 141 and 142 and floating electrodes 143 and 144, and has contact holes 157 and 158 exposing portions of the redundant gate lines 141 and 142. Accordingly, the gate lines 121 and 122 and the pixel electrode 190 are formed on the insulating layer 150, and the gate lines 121 and 122 are connected to the redundant gate lines 141 and 142 through the contact holes 157 and 158.

[90] Fig. 16 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention, and Fig. 17 is a sectional view of the thin film diode array panel taken along the line XVII-XVII of Fig. 16.

[91] When the thin film diode array panel of Figs. 16 and 17 is compared with that of Figs. 14 and 15, the shape of an insulating layer 150 is different.

[92] In the thin film diode array panel of Figs. 16 and 17, the insulating layer 150 has a cutout 159 disposed to overlap a portion of the pixel electrode 190 to enhance the light transmittance ratio.

[93] Furthermore, the number of contact holes 157 and 158 exposing the redundant gate lines 141 and 142 is increased to enhance the electrical connection between the redundant gate lines 141 and 142 and the gate lines 121 and 122.

[94] Fig. 18 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention.

[95] When the thin film diode array panel of Fig. 18 is compared with that of Figs. 14 and 15, the shape of an insulating layer 150 is different.

[96] The insulating layer 150 has a cutout 159 disposed under the main body of the pixel electrode 190 and exposing a portion of the insulating substrate 110 around the main

body of the pixel electrode 190 to enhance the light transmittance ratio.

[97] The insulating layer 150 has cutout stripes 157 and 158 exposing the redundant gate lines 141 and 142 to enhance the electrical connection between the redundant gate lines 141 and 142 and the gate lines 121 and 122.

[98] Fig. 19 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention, and Fig. 20 is a sectional view of the thin film diode array panel taken along the line XX-XX of Fig. 19.

[99] When the thin film diode array panel of Figs. 19 and 20 is compared with that of Figs. 8 and 9, the shape of an insulating layer 150 is different.

[100] That is, the insulating layer 150 is formed on the entire area of the insulating substrate 110 to cover the redundant gate lines 141 and 142 and contact electrodes 157 and 158. The insulating layer 150 has contact holes 157 and 158 exposing portions of the redundant gate lines 141 and 142, and contact holes 155 and 156 exposing a portion of the contact electrodes 147 and 148.

[101] Accordingly, the gate lines 121 and 122 and the pixel electrode 190 are formed on the insulating layer 150. The gate lines 121 and 122 are connected to the redundant gate lines 141 and 142 through the contact holes 157 and 158, and the pixel electrode 190 is connected to the contact electrodes 147 and 148 through the contact holes 155 and 156.

[102] Fig. 21 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention, and Fig. 22 is a sectional view of the thin film diode array panel taken along the line XXII-XXII of Fig. 21.

[103] When the thin film diode array panel of Figs. 21 and 22 is compared with that of Figs. 19 and 20, the shape of an insulating layer 150 is different.

[104] In the thin film diode array panel of Figs. 21 and 22, the insulating layer 150 has a cutout 159 disposed to overlap a portion of the pixel electrode 190 to enhance the light transmittance ratio.

[105] Furthermore, the number of contact holes 157 and 158 exposing the redundant gate lines 141 and 142 is increased to enhance the electrical connection between the redundant gate lines 141 and 142 and the gate lines 121 and 122.

[106] Fig. 23 is a layout view of a thin film diode array panel for a liquid crystal display according to another embodiment of the present invention.

[107] When the thin film diode array panel of Fig. 23 is compared with that of Figs. 19 and 20, the shape of an insulating layer 150 is different.

[108] The insulating layer 150 has a cutout 159 disposed under the main body of the pixel

electrode 190 and exposes a portion of the insulating substrate 110 around the main body of the pixel electrode 190 to enhance the light transmittance ratio.

[109] The insulating layer 150 has cutout stripes 157 and 158 exposing the redundant gate lines 141 and 142 to enhance the electrical connection between the redundant gate lines 141 and 142 and the gate lines 121 and 122.

[110] Although the illustrative embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the present invention is not limited to those precise embodiments, and that various changes and modifications may be affected therein by one of ordinary skill in the related art without departing from the scope or spirit of the invention. All such changes and modifications are intended to be included within the scope of the invention as defined by the appended claims.